FIG. 1

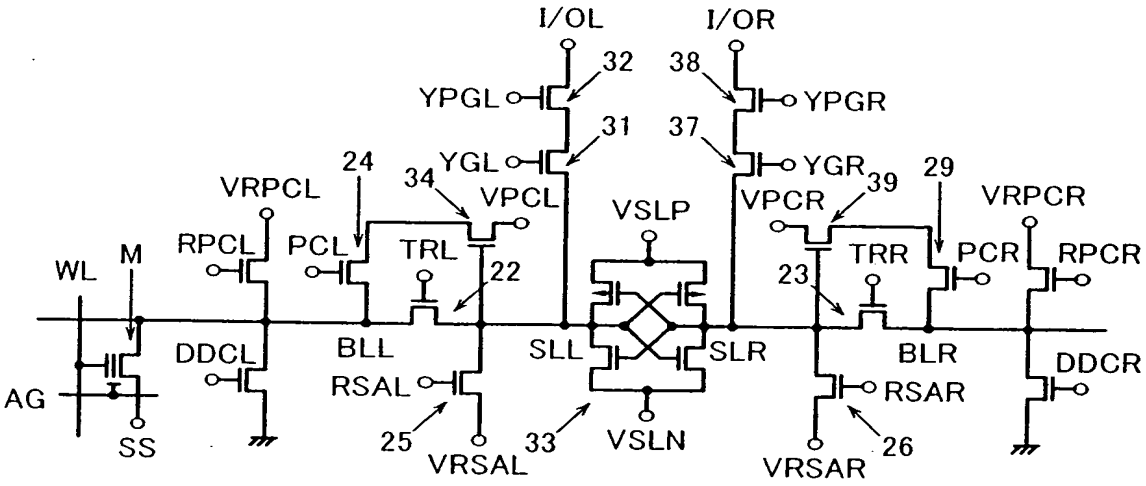

I/OL
I/OR
32
38
YPGL
YPGR
31
37
YGL
YGR
24
34
39
29
VRPCL
VPCL
VSLP
VPCR
VRPCR
RPCL
PCL
TRL
TRR
PCR
RPCR
WL
M
22
23
DDCL
BLL
SLL
SLR
BLR
DDCR
AG
RSAL
RSAR
SS
25
33
26
VRSAL
VSLN
VRSAR

FIG. 2

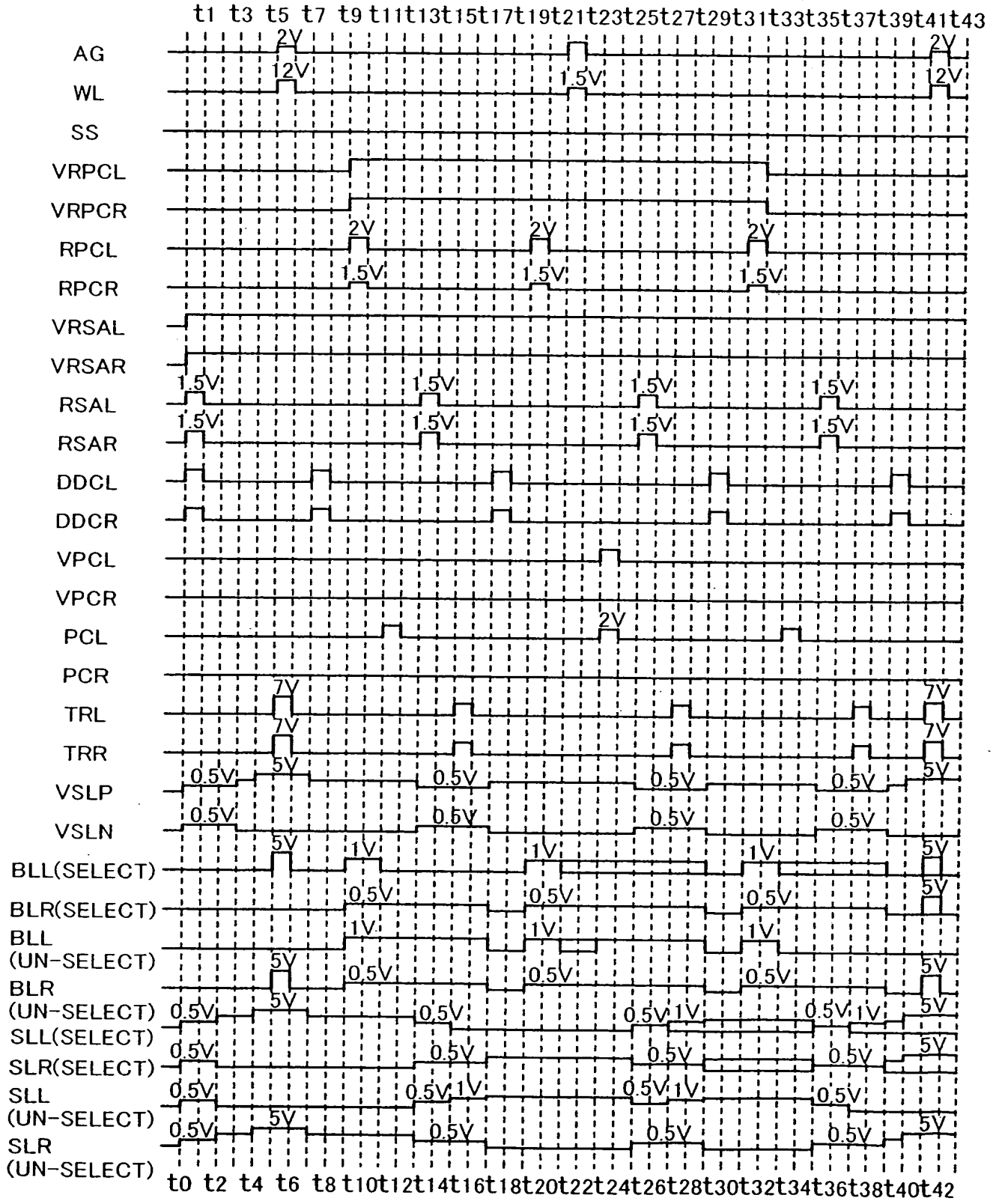

t1 t3 t5 t7 t9 t11 t13 t15 t17 t19 t21 t23 t25 t27 t29 t31 t33 t35 t37 t39 t41 t43
AG
WL
SS
VRPCL
VRPCR
RPCL
RPCR
VRSAL
VRSAR
RSAL
RSAR
DDCL
DDCR
VPCL
VPCR
PCL
PCR
TRL
TRR
VSLP
VSLN
BLL(SELECT)
BLR(SELECT)
BLL (UN-SELECT)
BLR (UN-SELECT)
SLL(SELECT)
SLR(SELECT)
SLL (UN-SELECT)
SLR (UN-SELECT)
t0 t2 t4 t6 t8 t10 t12 t14 t16 t18 t20 t22 t24 t26 t28 t30 t32 t34 t36 t38 t40 t42

FIG. 3

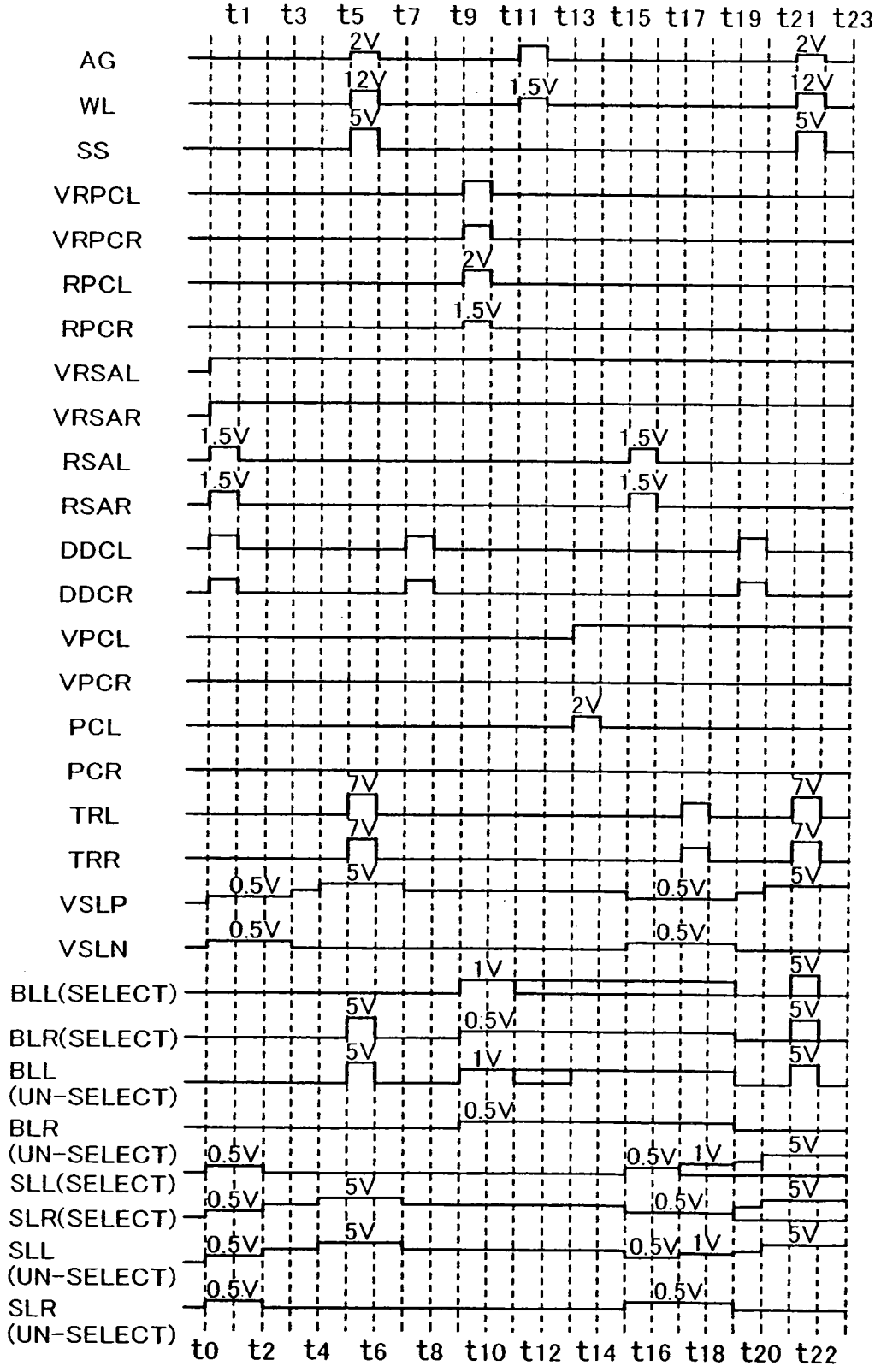

t1 t3 t5 t7 t9 t11 t13 t15 t17 t19 t21 t23
AG
WL
SS
VRPCL
VRPCR
RPCL
RPCR
VRSAL
VRSAR
RSAL
RSAR
DDCL
DDCR
VPCL
VPCR
PCL
PCR
TRL
TRR
VSLP
VSLN
BLL(SELECT)
BLR(SELECT)
BLL (UN-SELECT)
BLR (UN-SELECT)
SLL(SELECT)
SLR(SELECT)
SLL (UN-SELECT)
SLR (UN-SELECT)
2V
1.2V
5V
1.5V
7V
0.5V
1V
t0 t2 t4 t6 t8 t10 t12 t14 t16 t18 t20 t22

FIG. 4

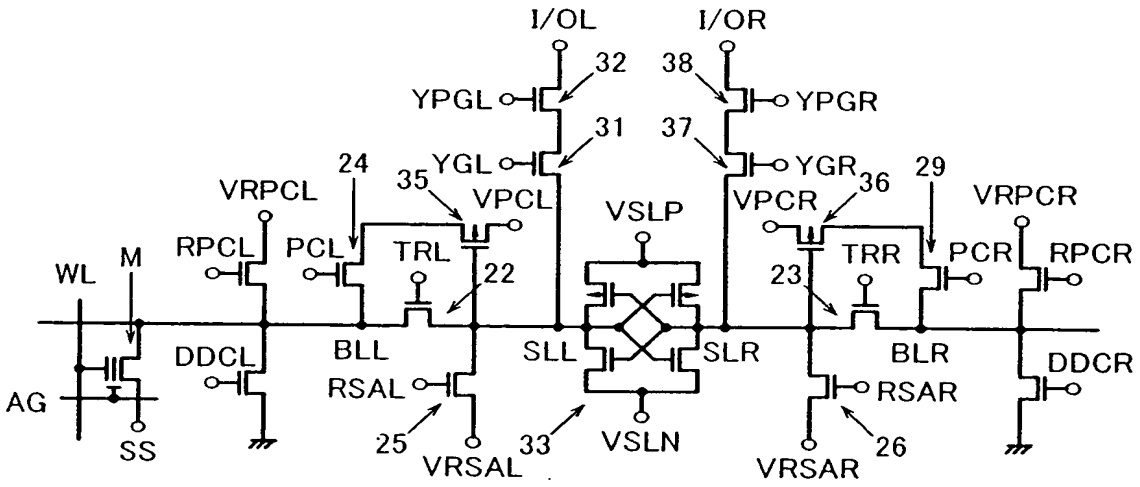

I/OL
I/OR
32
38
YPGL
YPGR
31
37
YGL
YGR
24
35
29
36
VRPCL
VPCL
VSLP
VPCR
VRPCR
RPCL
PCL
TRL
TRR
PCR
RPCR
WL
M
22
23
DDCL
BLL
SLL
SLR
BLR
DDCR
AG
RSAL
RSAR
SS
25
33
26
VRSAL
VSLN
VRSAR

FIG. 5

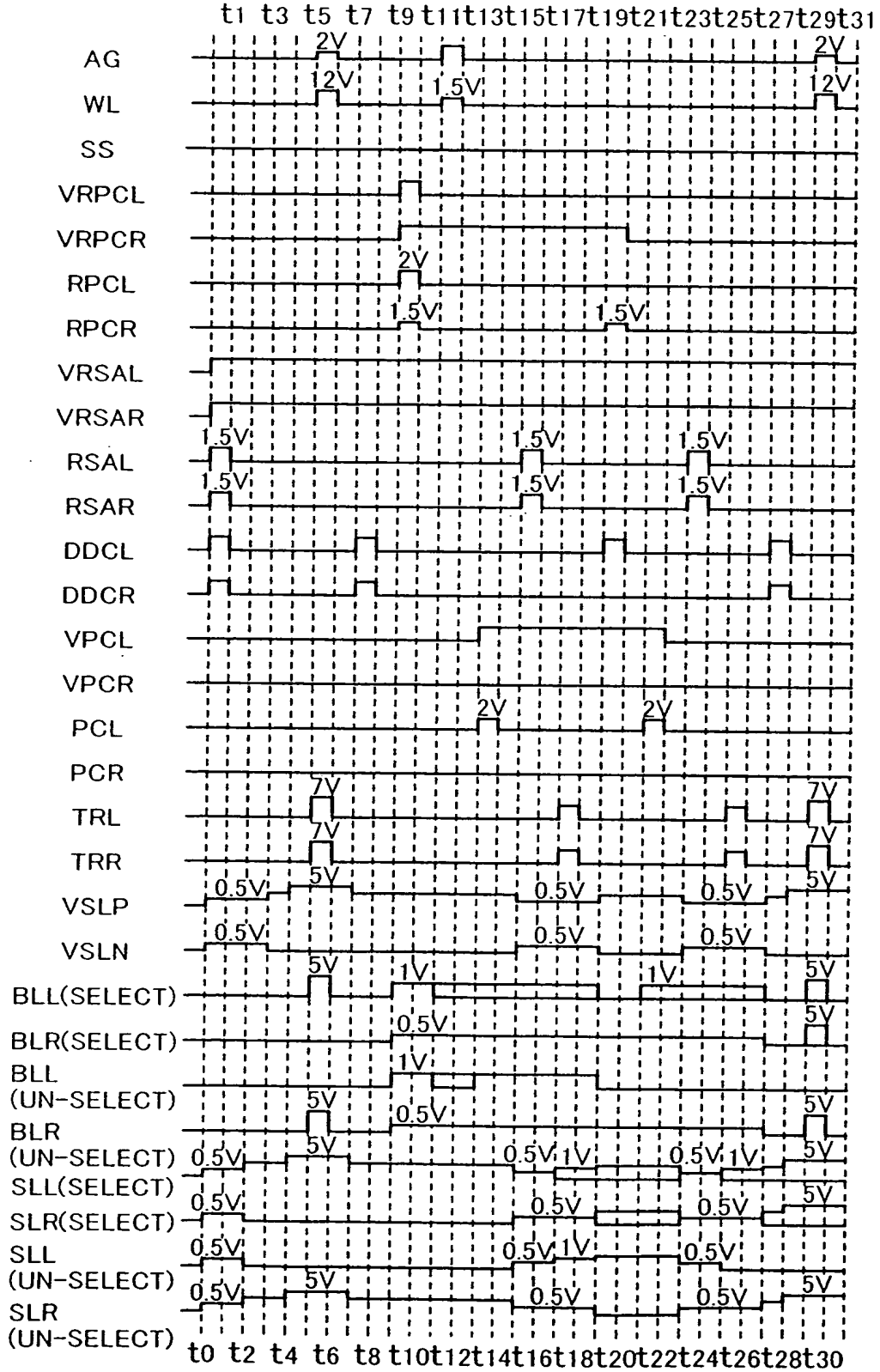

t1 t3 t5 t7 t9 t11 t13 t15 t17 t19 t21 t23 t25 t27 t29 t31
AG
WL
SS
VRPCL
VRPCR
RPCL
RPCR
VRSAL
VRSAR
RSAL
RSAR
DDCL
DDCR
VPCL
VPCR
PCL
PCR
TRL
TRR
VSLP
VSLN
BLL(SELECT)
BLR(SELECT)
BLL (UN-SELECT)
BLR (UN-SELECT)
SLL(SELECT)
SLR(SELECT)
SLL (UN-SELECT)
SLR (UN-SELECT)
2V
1.2V
1.5V
0.5V
1V
5V
7V
t0 t2 t4 t6 t8 t10 t12 t14 t16 t18 t20 t22 t24 t26 t28 t30

FIG. 6

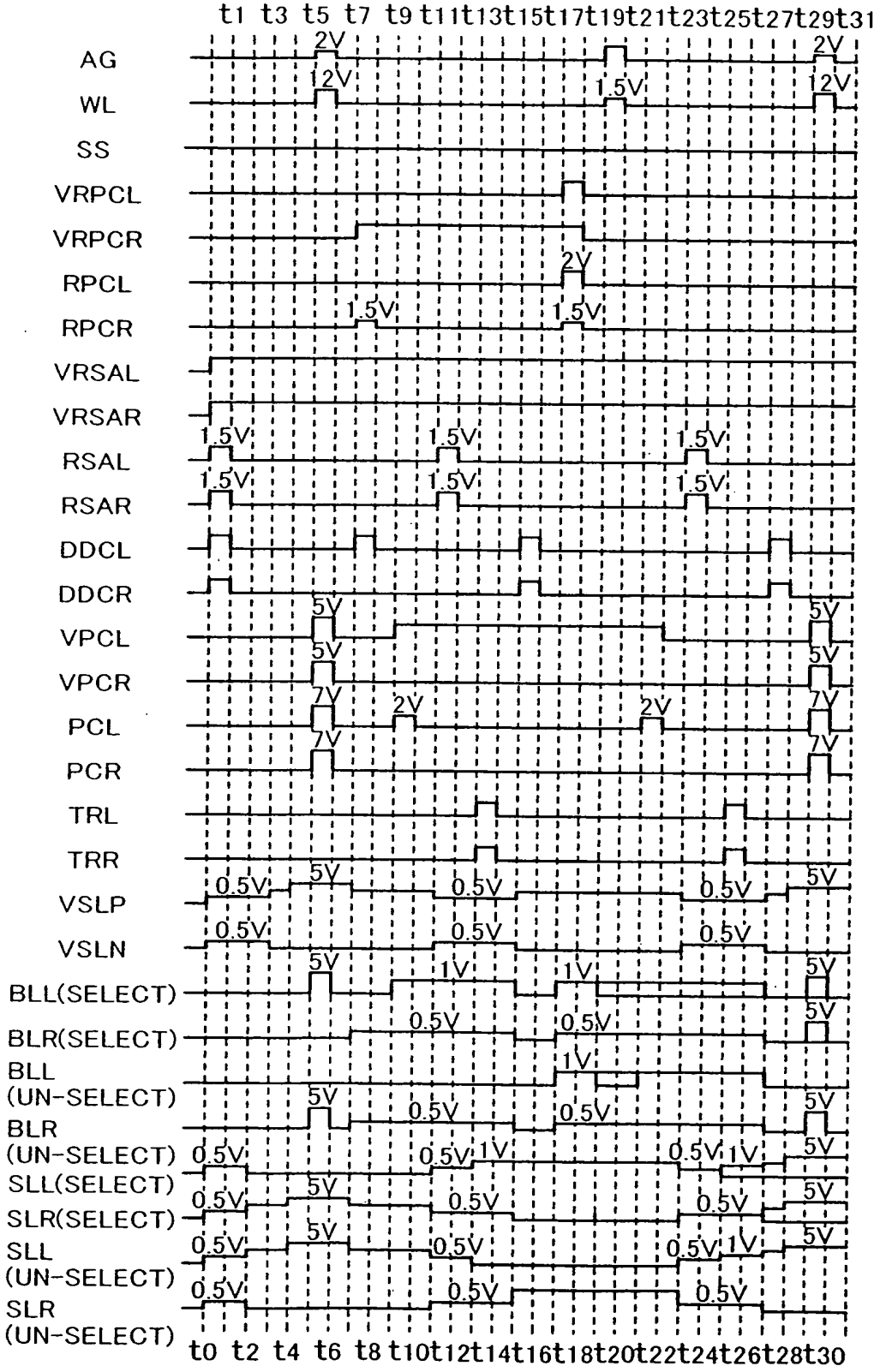

t1 t3 t5 t7 t9 t11 t13 t15 t17 t19 t21 t23 t25 t27 t29 t31
AG
WL
SS
VRPCL
VRPCR
RPCL
RPCR
VRSAL
VRSAR
RSAL
RSAR
DDCL
DDCR
VPCL
VPCR
PCL
PCR
TRL
TRR
VSLP
VSLN
BLL(SELECT)
BLR(SELECT)
BLL (UN-SELECT)
BLR (UN-SELECT)
SLL(SELECT)
SLR(SELECT)
SLL (UN-SELECT)
SLR (UN-SELECT)
t0 t2 t4 t6 t8 t10 t12 t14 t16 t18 t20 t22 t24 t26 t28 t30

FIG. 7

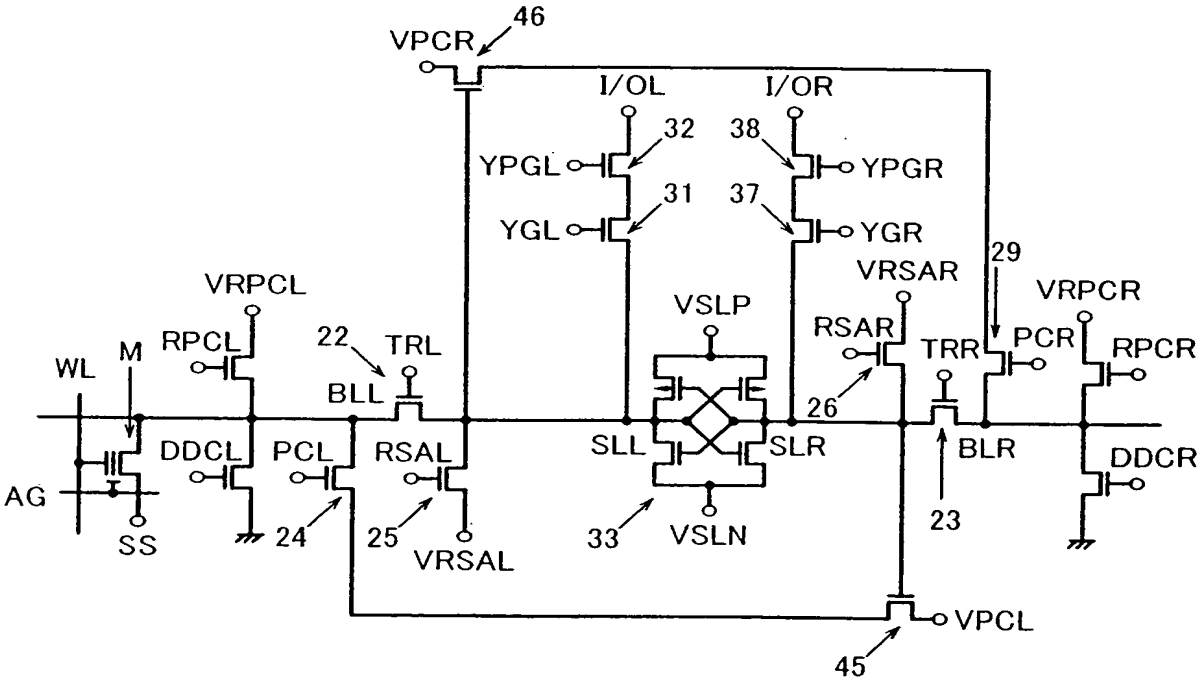

46
VPCR
I/OL
I/OR
32
38
YPGL
YPGR
31
37
YGL
YGR
29
VRSAR
VRPCR
VRPCL
VSLP
RSAR
PCR
RPCR
RPCL
22
TRL
TRR
WL
M
BLL
26
DDCL
PCL
RSAL
SLL
SLR
BLR
DDCR
AG
SS
24
25
VRSAL
33
VSLN
23
VPCL
45

FIG. 8

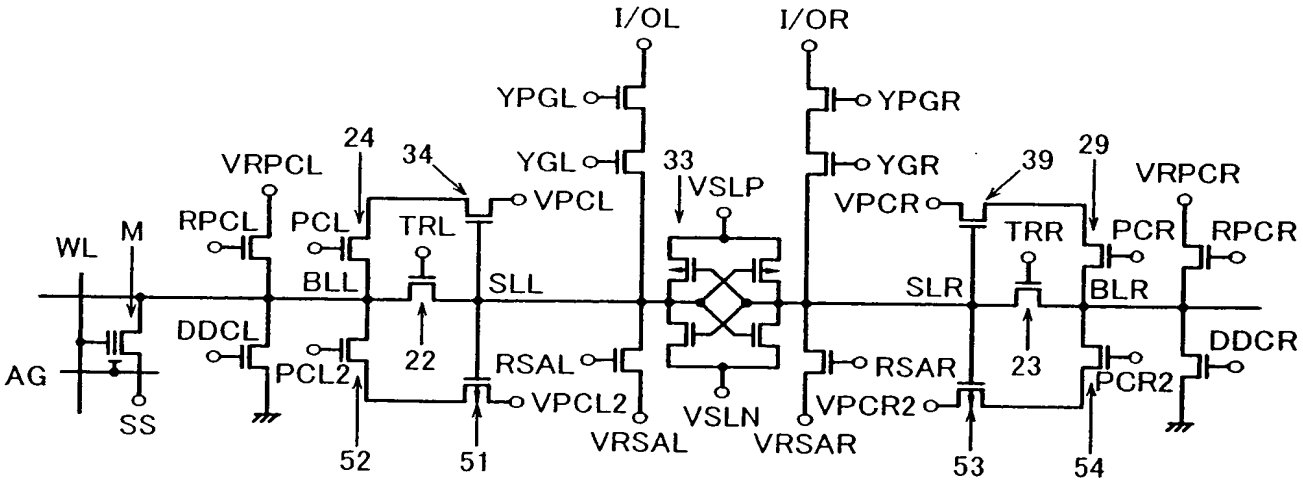

I/OL
I/OR
YPGL
YPGR
YGL
YGR
VRPCL
24
34
33
VSLP
39
29
VRPCR
VPCL
VPCR
RPCL
PCL
TRL
TRR
PCR
RPCR
WL
M
BLL
SLL
SLR
BLR
DDCL
DDCR
AG
22
23
PCL2
RSAL
RSAR
PCR2
VPCL2
VPCR2
SS
VSLN
VRSAL
VRSAR
52
51
53
54

FIG. 9

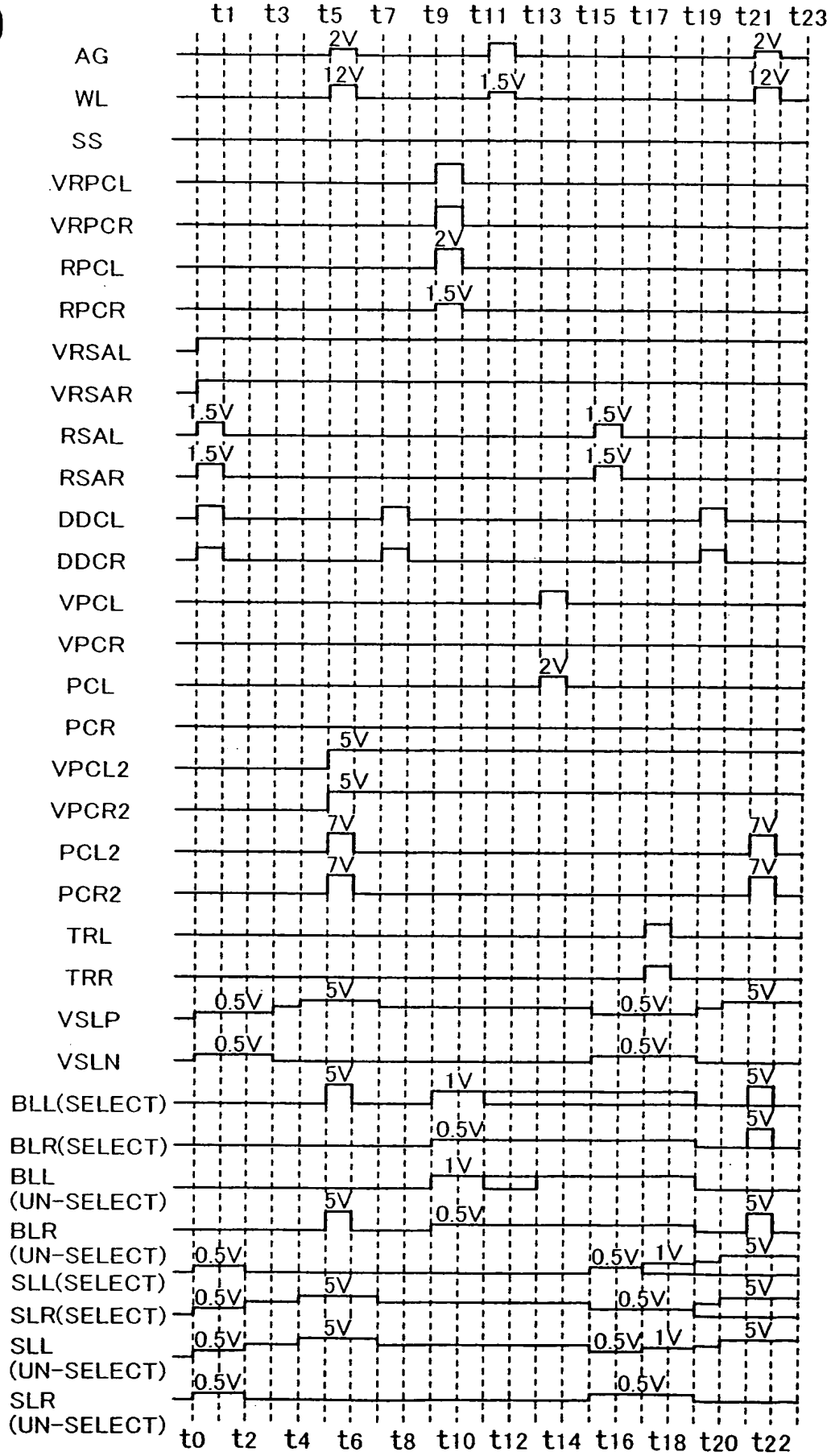

t1 t3 t5 t7 t9 t11 t13 t15 t17 t19 t21 t23
AG
WL
SS
VRPCL
VRPCR
RPCL
RPCR
VRSAL
VRSAR
RSAL
RSAR
DDCL
DDCR
VPCL
VPCR
PCL
PCR
VPCL2
VPCR2
PCL2
PCR2
TRL
TRR
VSLP
VSLN
BLL(SELECT)
BLR(SELECT)
BLL (UN-SELECT)
BLR (UN-SELECT)
SLL(SELECT)
SLR(SELECT)
SLL (UN-SELECT)
SLR (UN-SELECT)
2V
12V
1.5V
5V
7V
0.5V
1V
t0 t2 t4 t6 t8 t10 t12 t14 t16 t18 t20 t22

FIG. 10

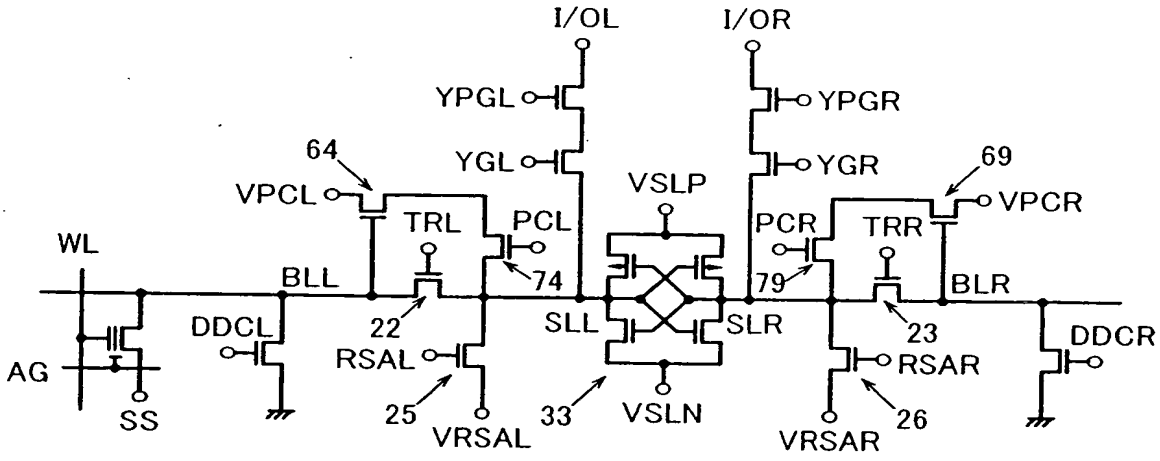

I/OL
I/OR
YPGL
YPGR
64
YGL
YGR
69
VSLP
VPCL
TRL
PCL
PCR
TRR
VPCR
WL
BLL
74
79
BLR
DDCL
22
SLL
SLR
23
DDCR
AG
RSAL
RSAR
SS
25
33
VSLN
26
VRSAL
VRSAR

FIG. 11

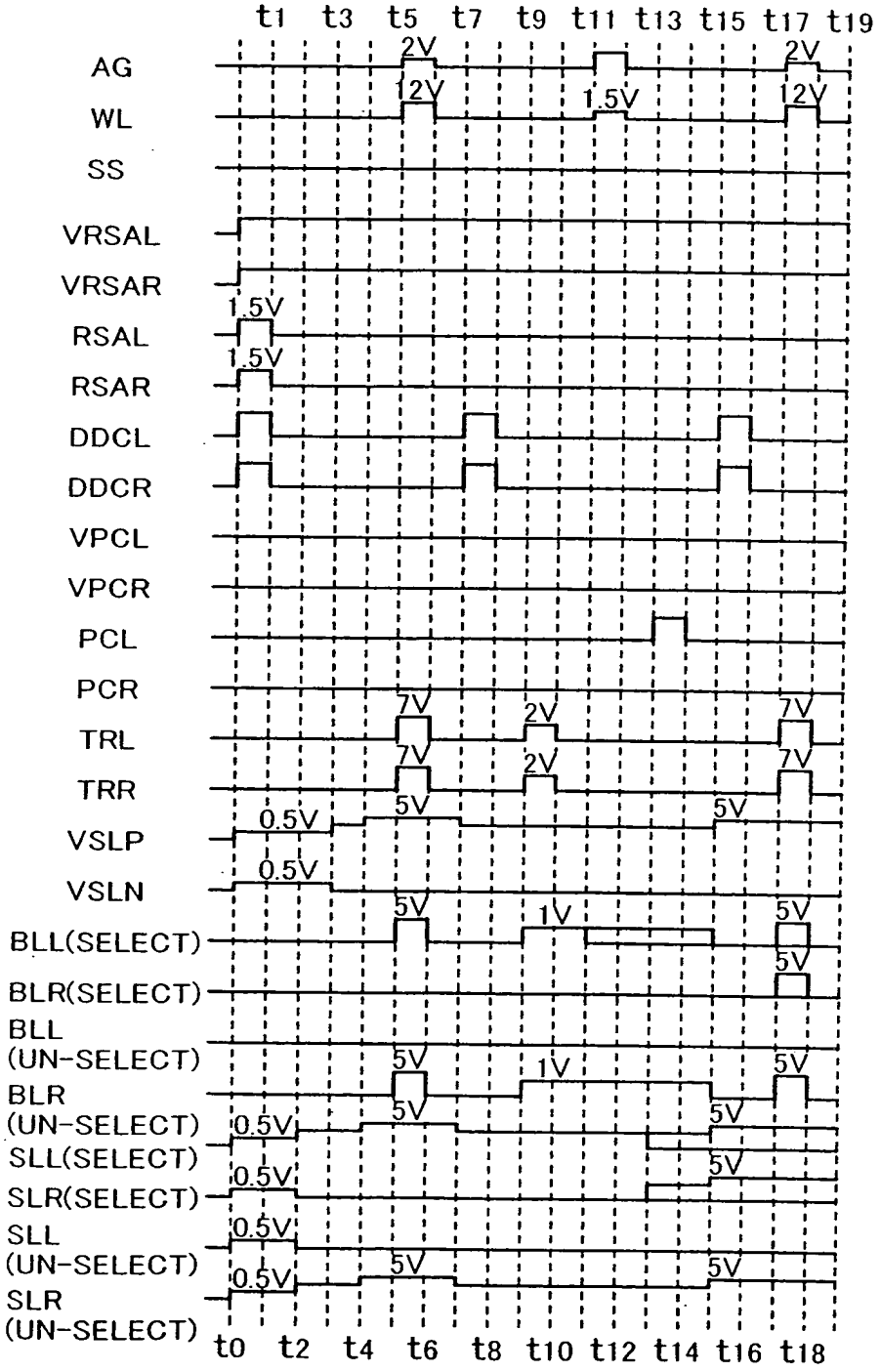

t1 t3 t5 t7 t9 t11 t13 t15 t17 t19
AG
WL
SS
VRSAL
VRSAR
RSAL
RSAR
DDCL
DDCR
VPCL
VPCR
PCL
PCR
TRL
TRR
VSLP
VSLN
BLL(SELECT)
BLR(SELECT)
BLL (UN-SELECT)
BLR (UN-SELECT)
SLL(SELECT)
SLR(SELECT)
SLL (UN-SELECT)
SLR (UN-SELECT)
2V
12V
1.5V
7V
5V
1V
0.5V
t0 t2 t4 t6 t8 t10 t12 t14 t16 t18

FIG. 12A

PROGRAMMING BIAS VOLTAGE OF SELECTED MEMORY CELL

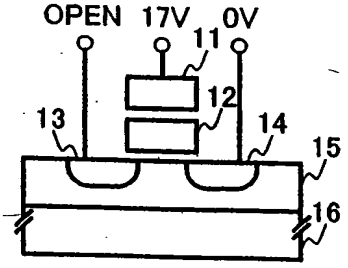


FIG. 12B

PROGRAMMING BIAS VOLTAGE OF UN-SELECTED MEMORY CELL

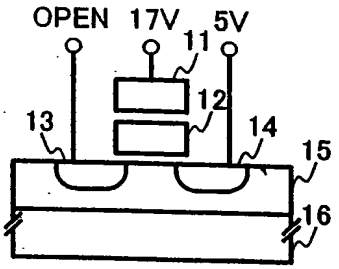


FIG. 13A

CURRENT SENSE AMPLIFIER

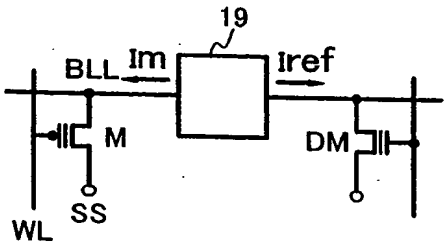


FIG. 13B

VOLTAGE SENSE AMPLIFIER

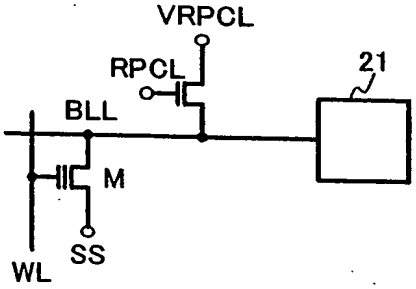


FIG. 14A

PROGRAMMING BIAS VOLTAGE OF SELECTED MEMORY CELL

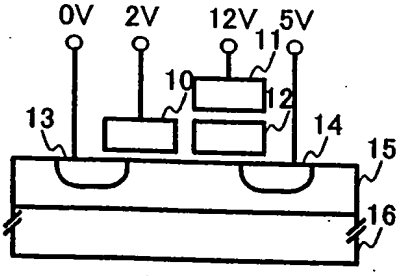


FIG. 14B

PROGRAMMING BIAS VOLTAGE OF UN-SELECTED MEMORY CELL

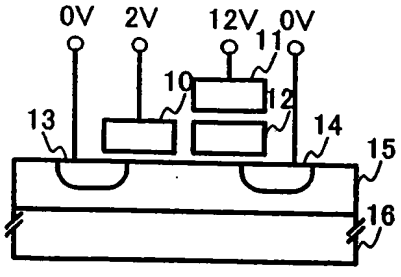


FIG. 15A

CIRCUIT DIAGRAM

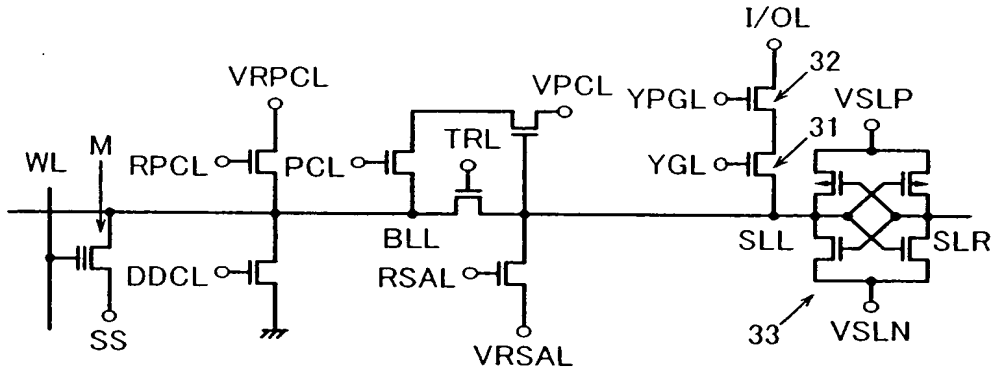


FIG. 15B

FLOW-CHART OF PROGRAMMING/VERIFICATION

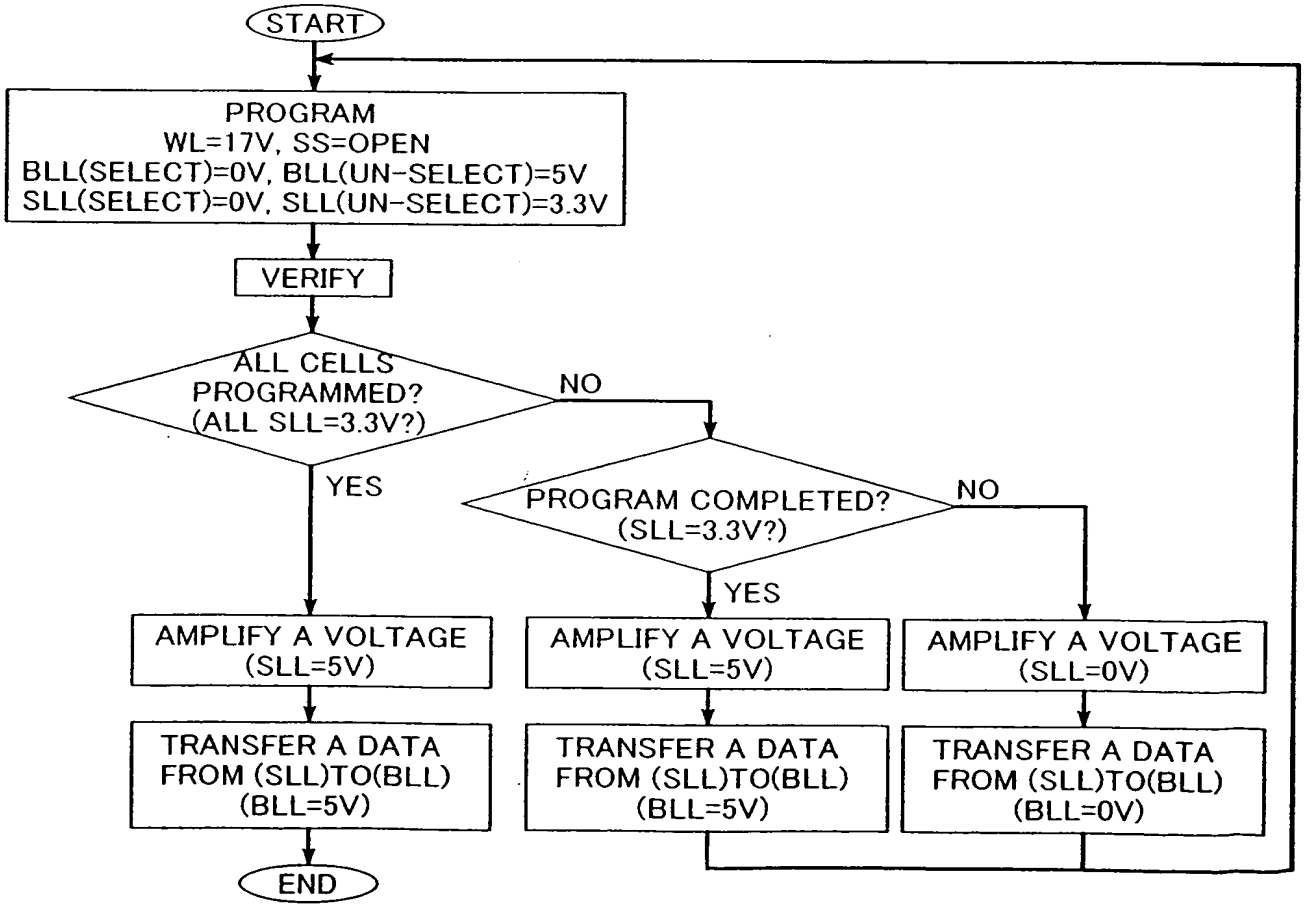


FIG. 16

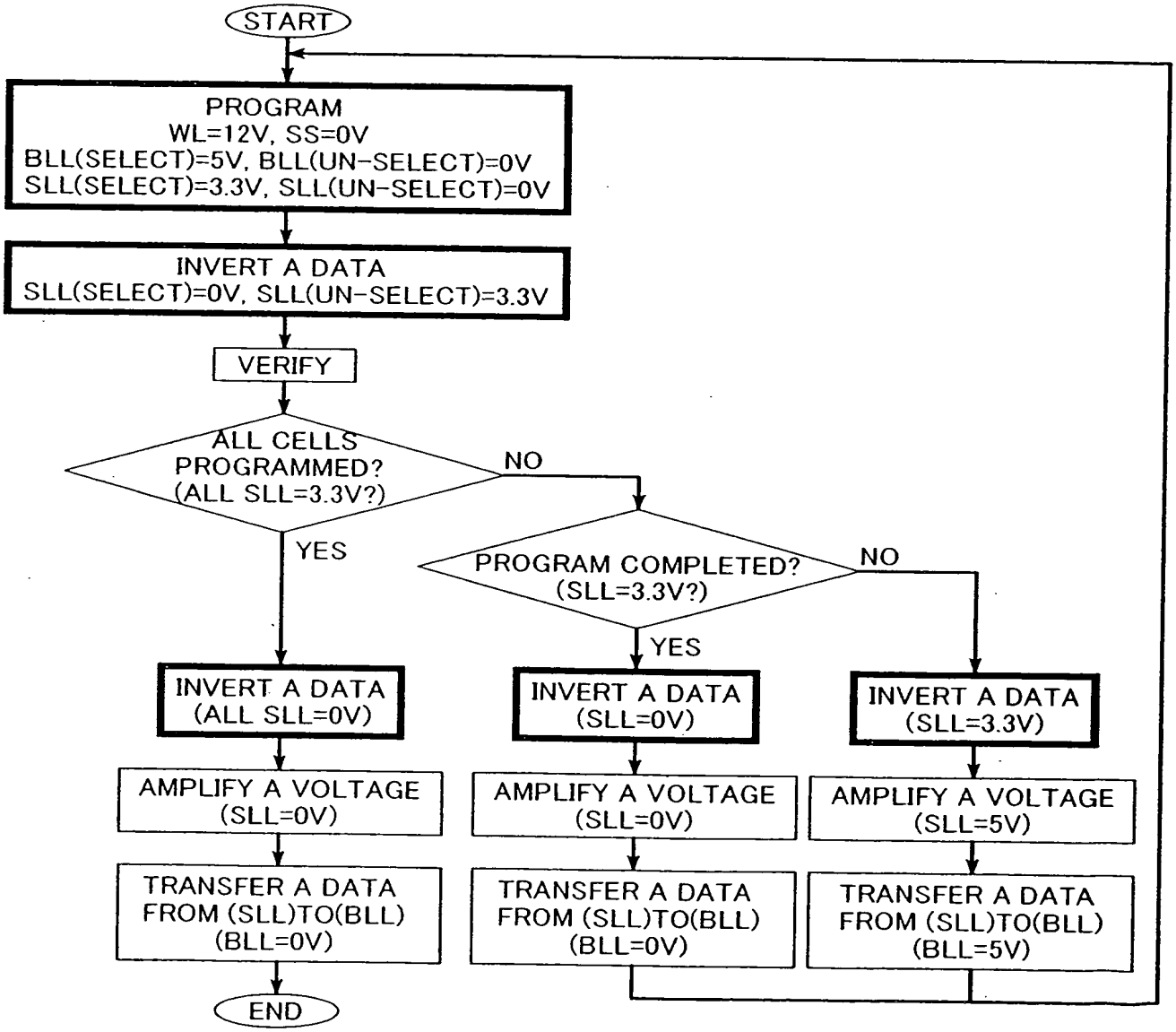

START
PROGRAM
WL=12V, SS=0V
BLL(SELECT)=5V, BLL(UN-SELECT)=0V
SLL(SELECT)=3.3V, SLL(UN-SELECT)=0V
INVERT A DATA
SLL(SELECT)=0V, SLL(UN-SELECT)=3.3V
VERIFY
ALL CELLS PROGRAMMED? (ALL SLL=3.3V?)
NO
YES
PROGRAM COMPLETED? (SLL=3.3V?)
NO
YES
INVERT A DATA (ALL SLL=0V)
INVERT A DATA (SLL=0V)
INVERT A DATA (SLL=3.3V)
AMPLIFY A VOLTAGE (SLL=0V)
AMPLIFY A VOLTAGE (SLL=0V)
AMPLIFY A VOLTAGE (SLL=5V)
TRANSFER A DATA FROM (SLL)TO(BLL) (BLL=0V)
TRANSFER A DATA FROM (SLL)TO(BLL) (BLL=0V)
TRANSFER A DATA FROM (SLL)TO(BLL) (BLL=5V)
END

FIG. 17A

TWO-LEVEL STORAGE

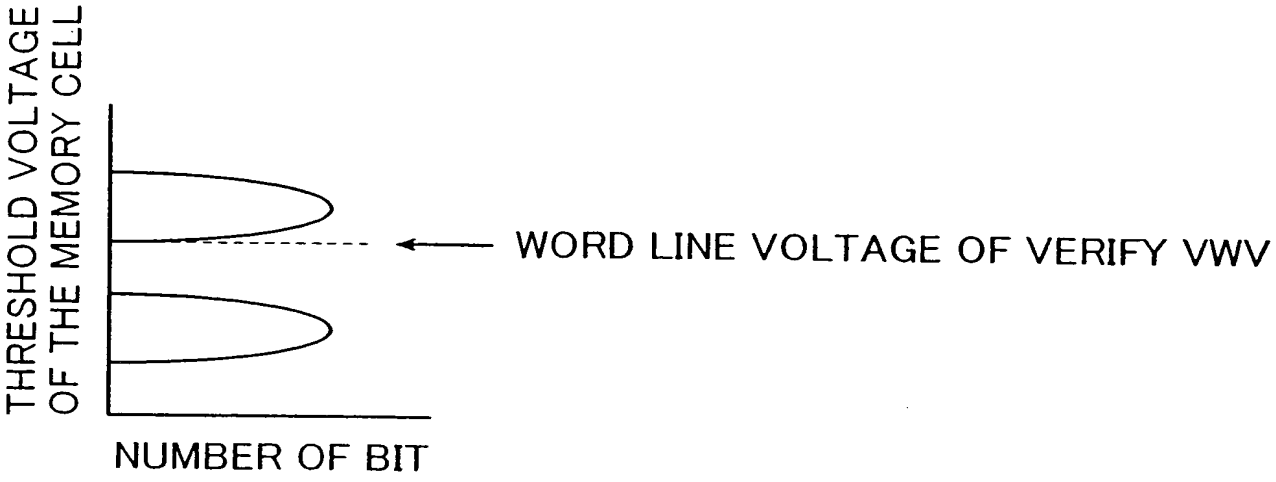


FIG. 17B

MULTI-LEVEL (FOUR-LEVEL) STORAGE

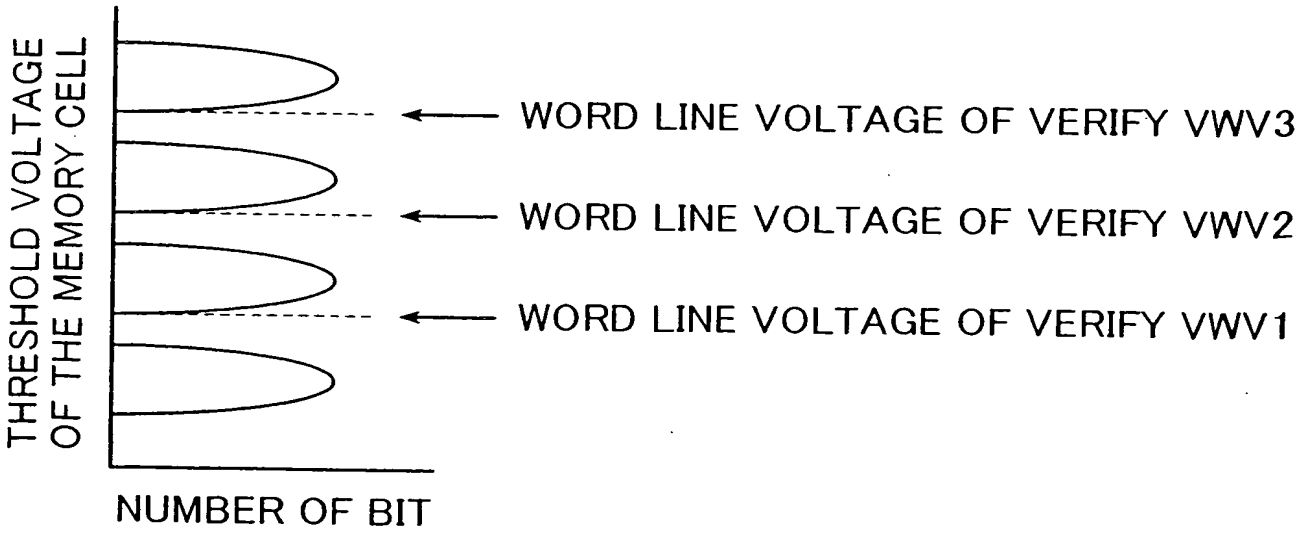


FIG. 18

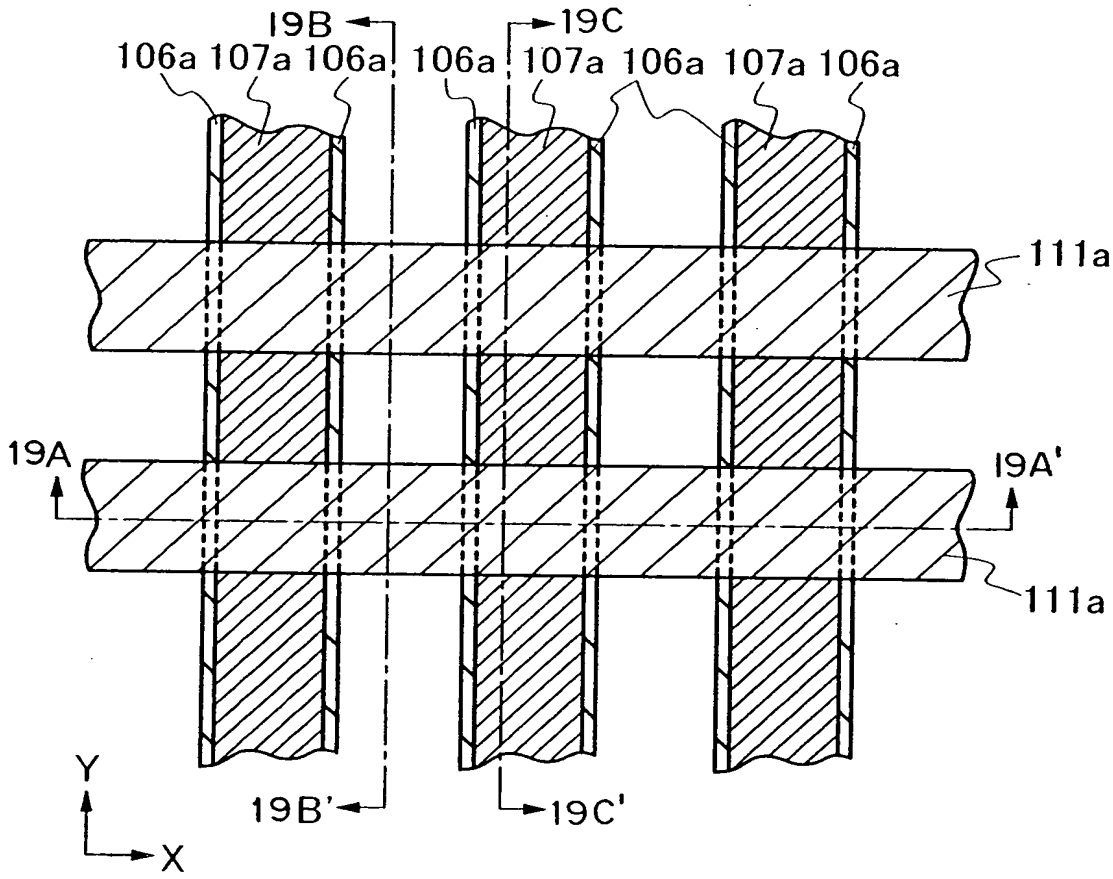

19B
19C
106a 107a 106a
106a 107a 106a 107a 106a
111a
19A
19A'
111a
Y
X
19B'
19C'

FIG. 19A

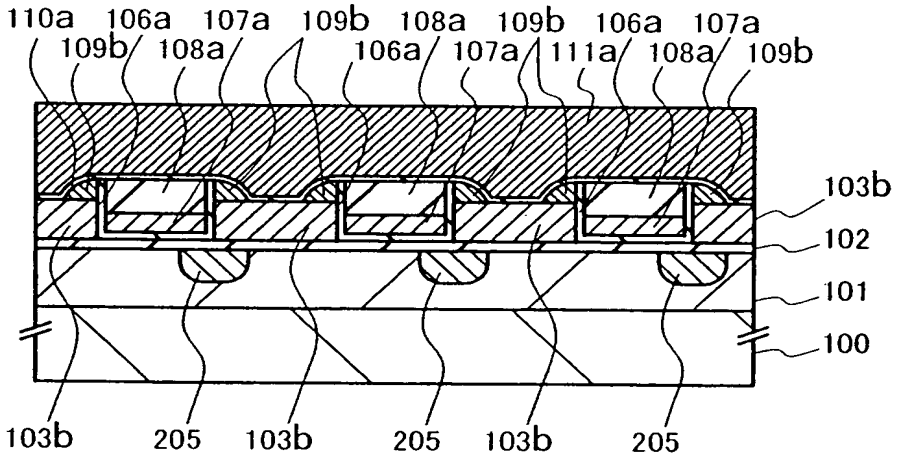


FIG. 19B

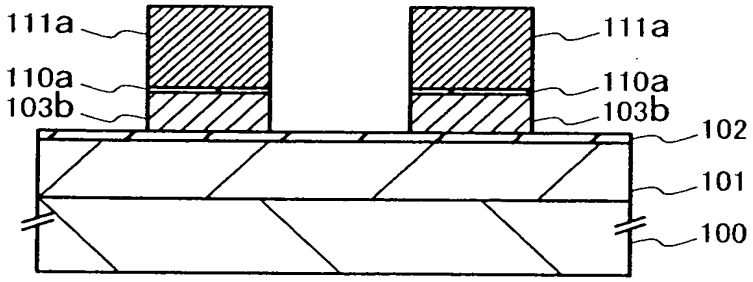


FIG. 19C

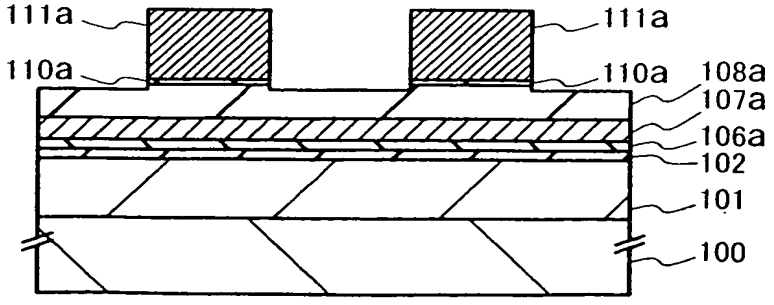


FIG. 20

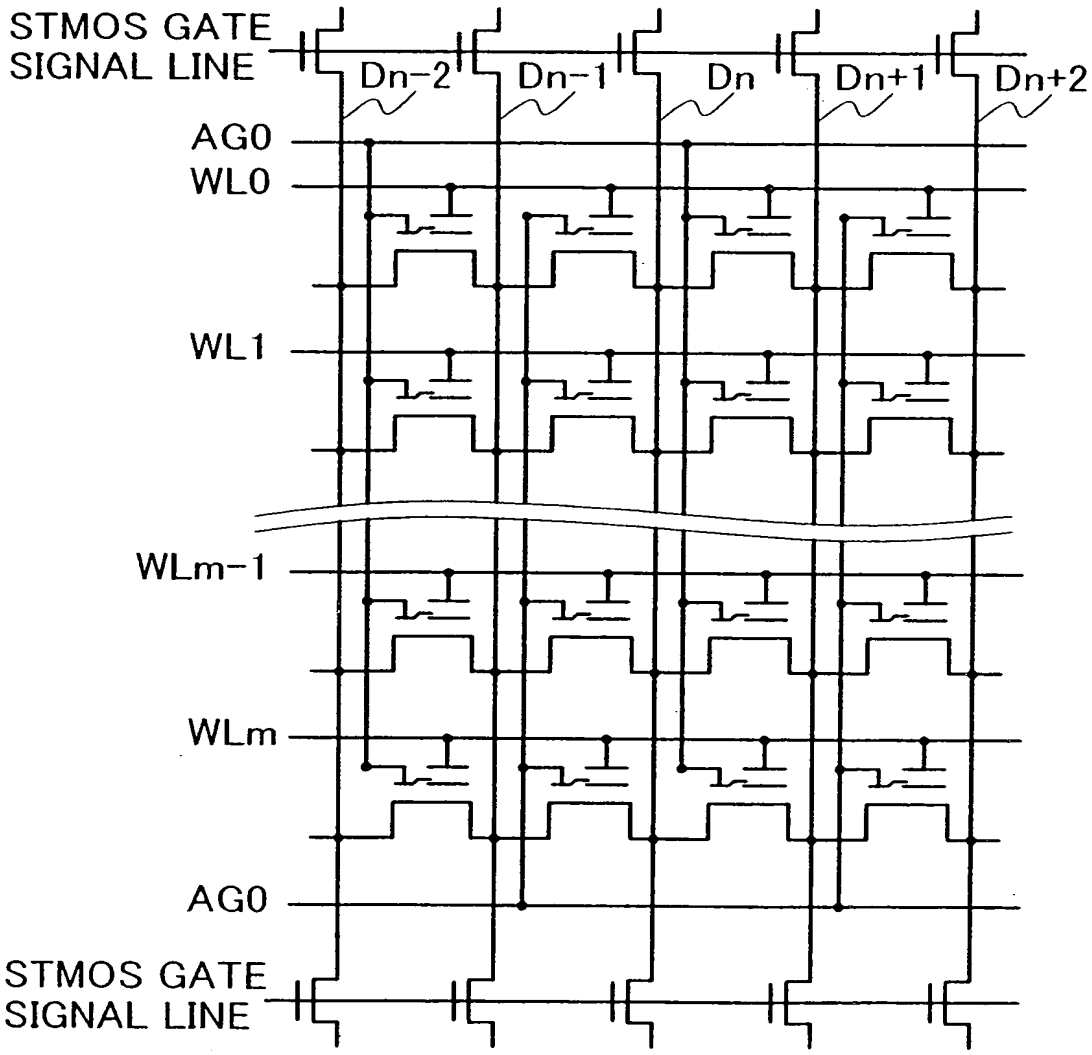

STMOS GATE SIGNAL LINE
Dn-2
Dn-1
Dn
Dn+1
Dn+2
AG0
WL0
WL1
WLm-1
WLm
AG0
STMOS GATE SIGNAL LINE

FIG. 21

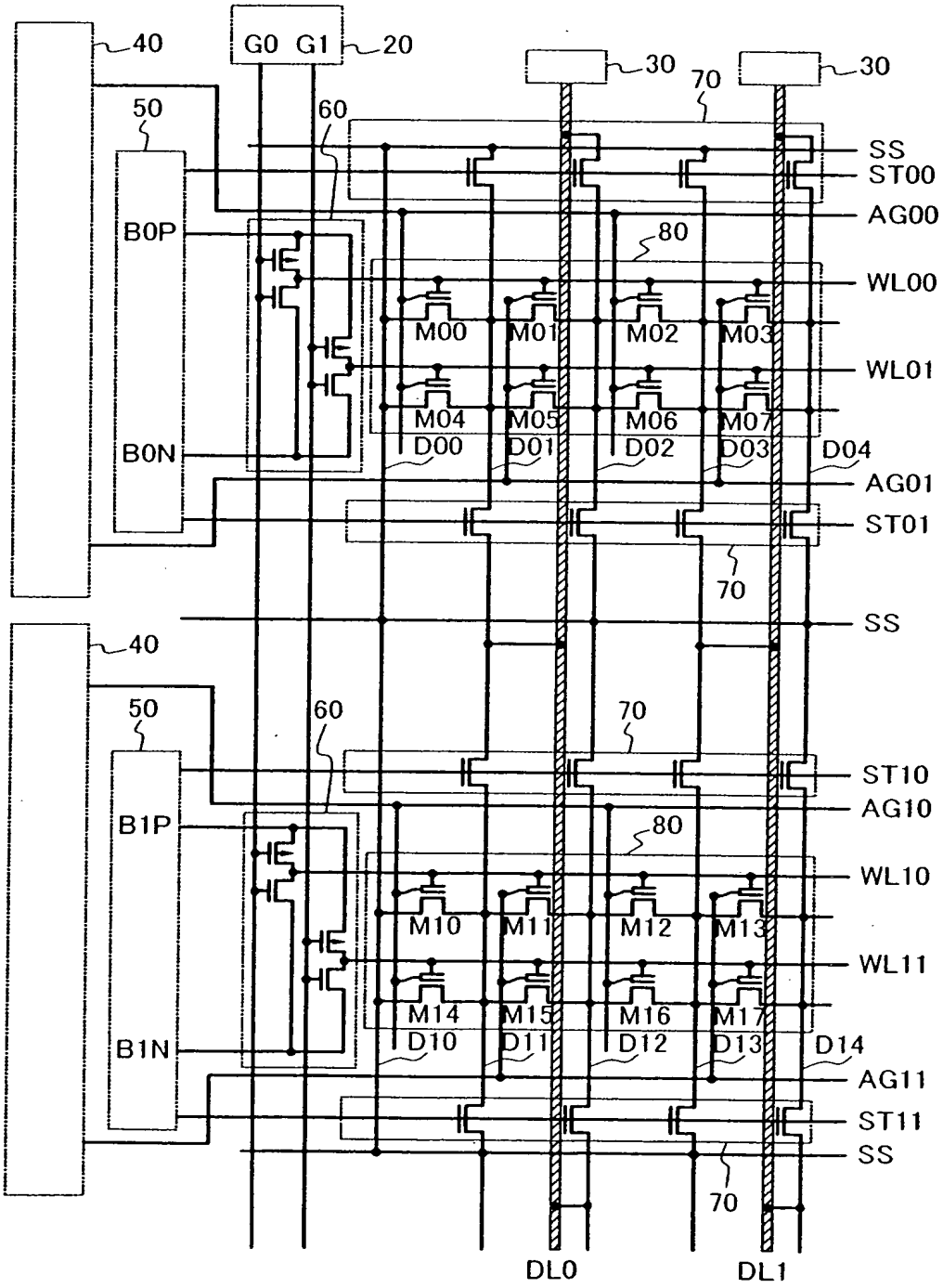
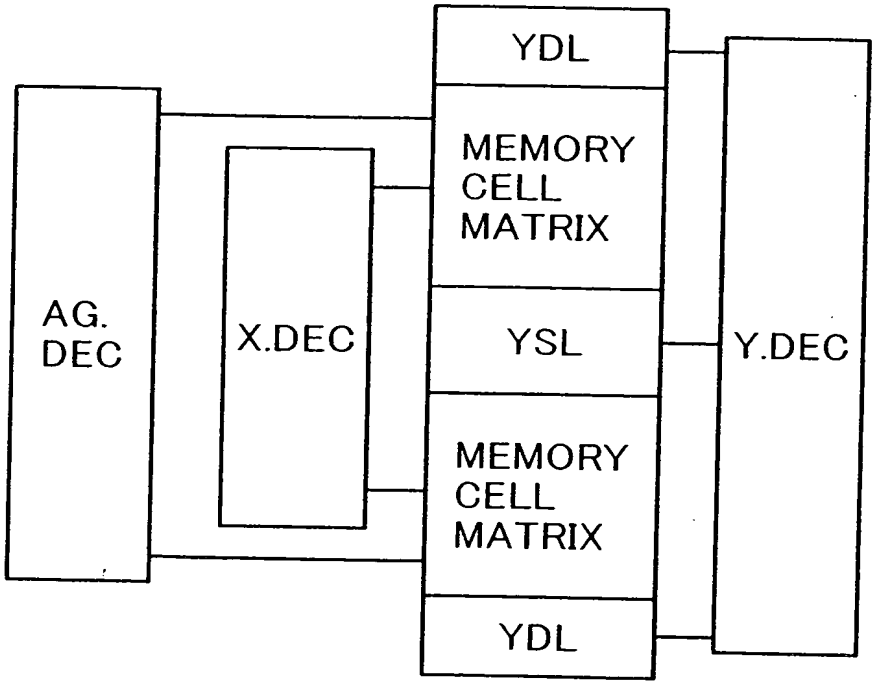

40
G0 G1
20
30
70
30
50
60
SS
ST00
AG00
B0P
80
WL00
M00
M01
M02
M03
WL01
M04
M05
M06
M07
B0N
D00
D01
D02
D03
D04
AG01
ST01
70
SS
40
50
60
70
ST10
AG10
B1P
80
WL10
M10
M11
M12
M13
WL11
M14
M15
M16
M17
B1N
D10
D11
D12
D13
D14
AG11
ST11
SS
70
DL0
DL1

FIG. 22


YDL
MEMORY CELL MATRIX
YSL
MEMORY CELL MATRIX
YDL
AG. DEC
X.DEC
Y.DEC